# A GaAs MONOLITHIC TRUE LOGARITHMIC AMPLIFIER FOR 0.5 TO 4 GHZ APPLICATIONS

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## ABSTRACT

A GaAs monolithic dual-gain amplifier stage for 0.5 to 4 GHz logarithmic amplifier applications has been developed and tested. A cascade of six of these stages has resulted in a true logarithmic amplifier with 70 dB dynamic range, operational across this band.

## INTRODUCTION

Logarithmic amplifiers are useful for compressing the dynamic range of signals prior to detection, so that detectors with limited dynamic range may be used in receiving systems to measure widely varying input signal amplitudes. Many types of logarithmic amplifiers have been developed (1), (2), and the type which is used in any particular application is determined by the system requirements. One type of logarithmic amplifier which is commonly used in systems which must perform signal processing functions on the phase of the incident signal is termed the true logarithmic amplifier. In the case of the true logarithmic amplifier, the output is a carrier frequency signal with voltage amplitude directly proportional to the logarithm of the input power level. An excellent explanation of the theory and design of the true logarithmic amplifier is found in (3); only a brief overview is presented here.

## THE TRUE LOGARITHMIC AMPLIFIER

The true logarithmic amplifier is composed of a cascade of dual-gain stages, as shown in Figure 1. Each stage contains two independent amplifiers which share a common input. One amplifier has high gain and a low limiting power level, and the other has unity gain and a high compression point. When the outputs of these two paths are combined, the result is an amplifier stage with an abrupt change in gain at some input power level. The stage has moderate gain (typically 10 dB) at low power levels, and gain approaching unity at higher power levels. Referring again to Figure 1, the case of 10 dB gain stages requires a voltage gain A of 2.16 or 6.7 dB to be combined with the unity gain arm. An amplifier comprised of a cascade of these stages will possess an output versus input characteristic which is a piecewise linear approximation to the desired logarithmic function.

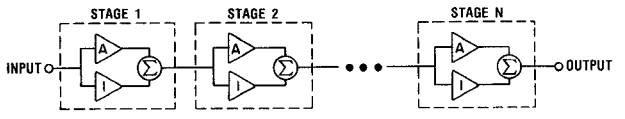


**Figure 1. Block Diagram of a True Logarithmic Amplifier.**

Excellent results have been obtained by constructing dual-gain stages as monolithic silicon amplifiers using bipolar transistors (4). Many companies are now producing true logarithmic amplifiers using these techniques. Typical of these implementations is a bandwidth of a few hundred MHz centered in the VHF or UHF frequency range.

## DESIGN

In this effort, the advantages of GaAs monolithic technology have been utilized to develop a monolithic dual-gain stage for the 0.5 to 4 GHz band. A schematic diagram of the circuit is shown in Figure 2. A stage gain of 10 dB was chosen, but because a −6 dB resistive combiner was used rather than an ideal combiner, the gains of both amplifier arms were increased 6 dB. The first arm has 12.7 dB gain and a saturated output power of −8 dBm, and the second arm has 6 dB gain and a saturated output power of +11 dBm. A thin film network external to the monolithic circuit contains the −6 dB resistive combiner in which the outputs of the two amplifier arms are combined to provide the linear gain of 10 dB at low power levels. Because of the low limiting power level in the higher gain arm, the gain of the stage begins to decrease as input power exceeds −20 dBm. The stage gain asymptotically approaches 0 dB as input power is further increased. Additional circuit elements printed on the thin film network are two shorted stubs which may be used for gain shaping and one series transmission line to equalize the insertion phase between the two paths.

Figure 3 is a photograph of the GaAs monolithic dual-gain amplifier. The circuit contains seven FET's, 29 GaAs resistors, and 18 capacitors for a total of 190 pF capacitance. The dimensions of the chip are 2.0 x 2.2 mm, and the thickness is 0.1 mm. Harmonic



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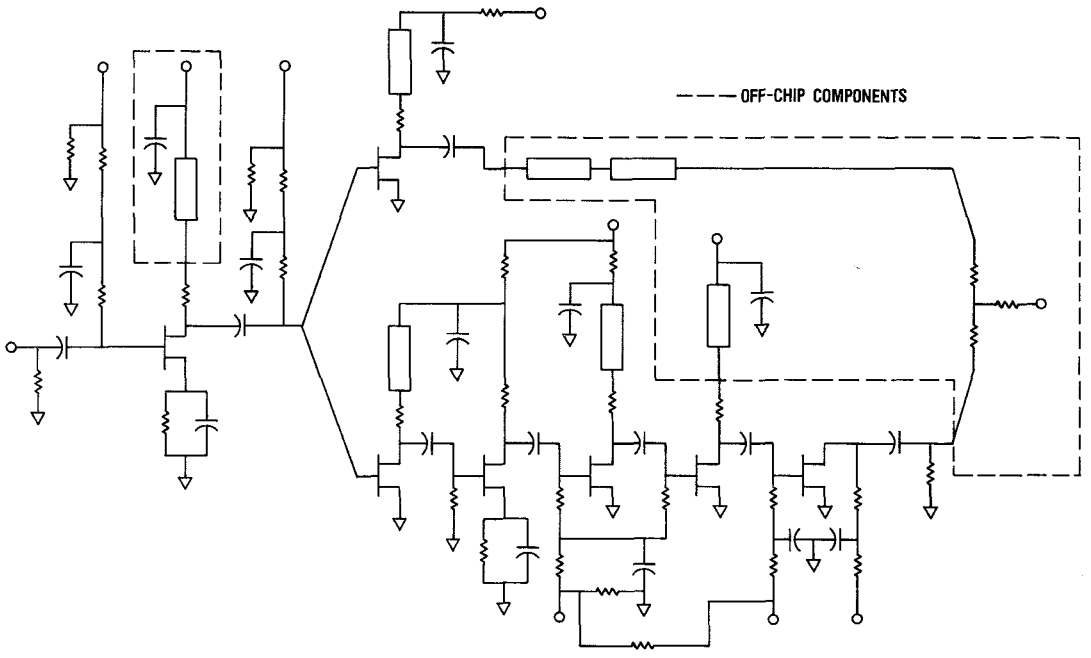


**Figure 2. Schematic Diagram of one Dual-Gain Stage.**

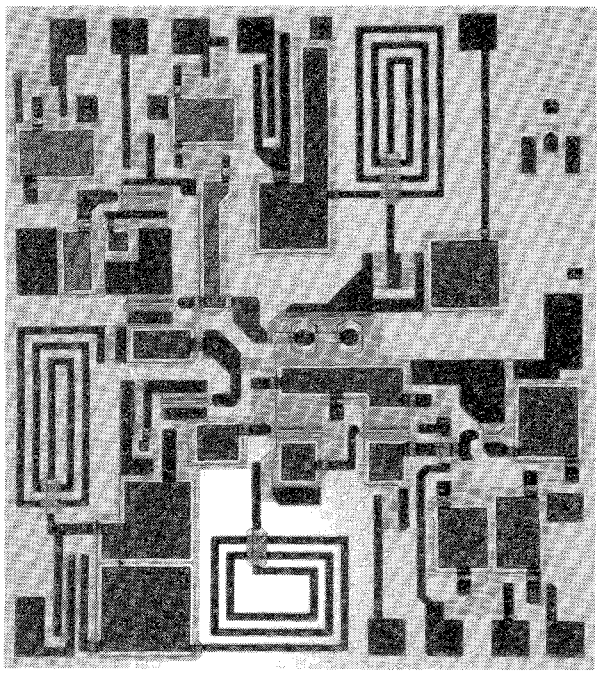

**Figure 3. Monolithic Dual-Gain Amplifier Chip.**

balance nonlinear analysis techniques were used to predict the compression point and saturated output power of each amplifier arm. This information was used to select a 50μm gate width FET for the output stage of the high gain arm and a 300μm FET for the output stage of the lower gain, higher compression point arm. All other FET's are of 150 μm gate width. A complete gain stage consists of the amplifier chip and its associated thin-film network mounted on a carrier plate, as seen in Figure 4.

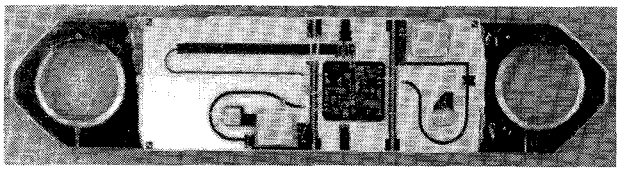

**Figure 4. Complete Dual-Gain Stage.**

## MEASURED PERFORMANCE

The measured voltage gain of one dual-gain amplifier stage is seen in Figure 5. The axes are scaled in peak volts to show the knee in the gain response which is characteristic of true logarithmic gain stages. Below the knee the slope is indicative of 10 dB linear gain, and above the knee the gain slope is unity until the lower gain amplifier eventually saturates.

Figure 6 is a picture of the six stage logarithmic amplifier composed of these dual-gain amplifier stages. Regulation for dc voltages is included in the housing. Power requirements are +8 V at 0.6 A and −8 V at 50 mA. The overall response of the amplifier is seen in Figure 7. At any given frequency in the 0.5 to 4 GHz band, the logarithmic error from a best fit line is less than ± 3.5 dB across input power levels between −70 and 0 dBm. The circuit exhibits some unexpected and undesirable peaking in gain at 1 GHz, as indicated by the higher logarithmic gain slope at this frequency.

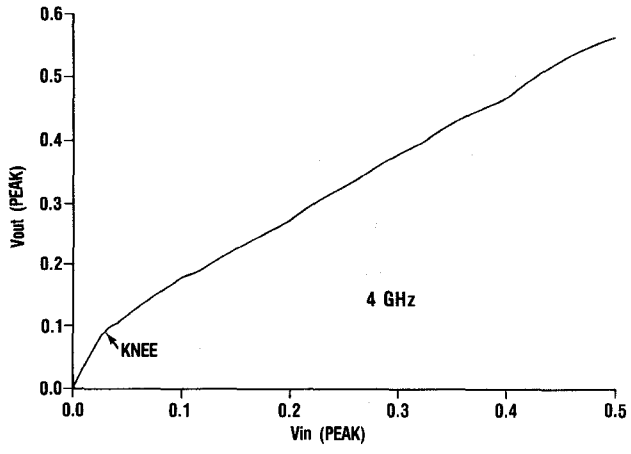


**Figure 5. Voltage Gain Characteristics of one Dual-Gain Stage.**

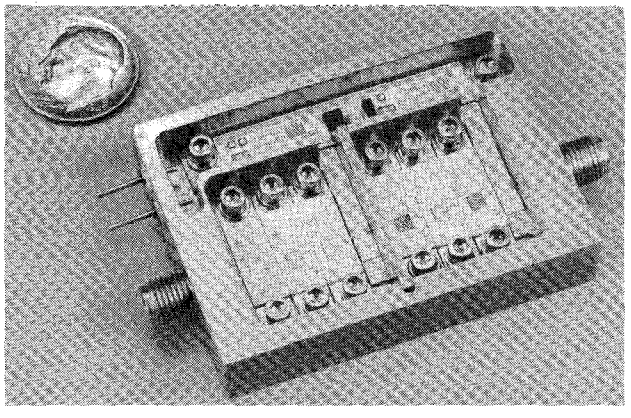

**Figure 6. Six-Stage True-Logarithmic Amplifier Module.**

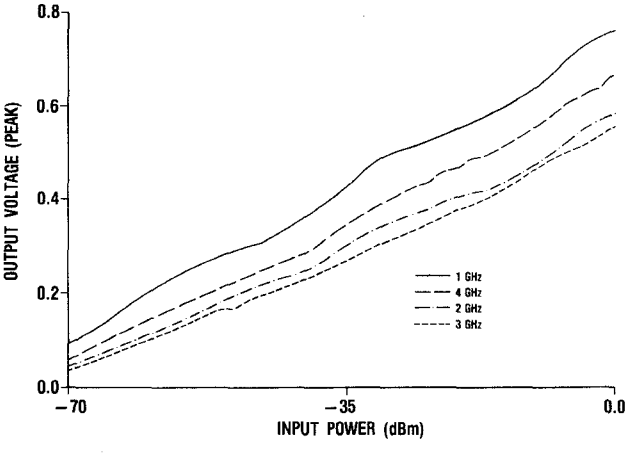


**Figure 7. Broadband Logarithmic Amplifier Response.**

Subsequent iterations of this component will be designed with greater emphasis on tolerance to process variation.

In system applications, it is desirable to select a frequency band such that the harmonics of the input frequency can never fall in band. If a band of 2 to 3 GHz is chosen, and the lengths of the gain shaping stubs on the thin film network are adjusted to yield the best amplifier performance within this band, the response of Figure 8 results. In this case, less than ± 5 dB error from a single best fit line is seen across frequency and powers between −70 and 0 dBm.

Insertion phase invariance as a function of input power level is another important performance parameter for a true logarithmic type amplifier. For the full bandwidth of 0.5 to 4 GHz, measured data indicate a maximum phase change of 14.5 degrees for any 10 dB power increment in the −70 to 0 dBm range, and a maximum error from an average insertion phase of 27 degrees for any frequency and power level in these ranges.

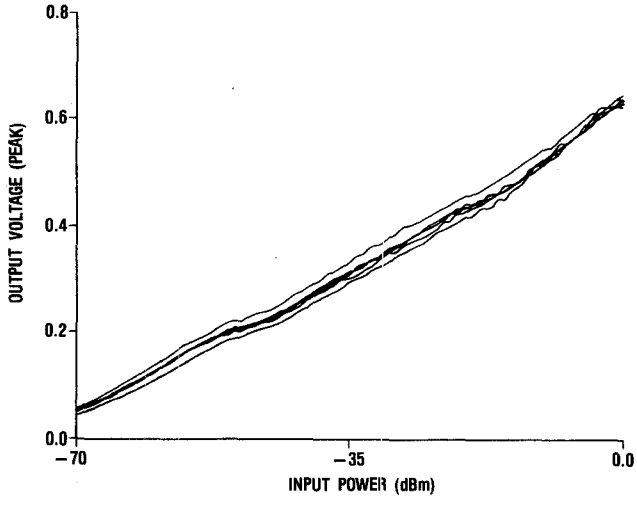


**Figure 8. Logarithmic Amplifier Response over 2 to 3 GHz Band. (Six curves have been plotted, corresponding to 200 MHz steps.)**

## CONCLUSION

In conclusion, a monolithic GaAs dual-gain amplifier circuit has been developed, and a logarithmic amplifier utilizing a cascade of these devices has been designed, built, and tested. The amplifier exhibits 70 dB dynamic range, and is operational over the 0.5 to 4 GHz band. This wide bandwidth will be useful in increasing the instantaneous information bandwidth of future microwave systems.

## ACKNOWLEDGMENT

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